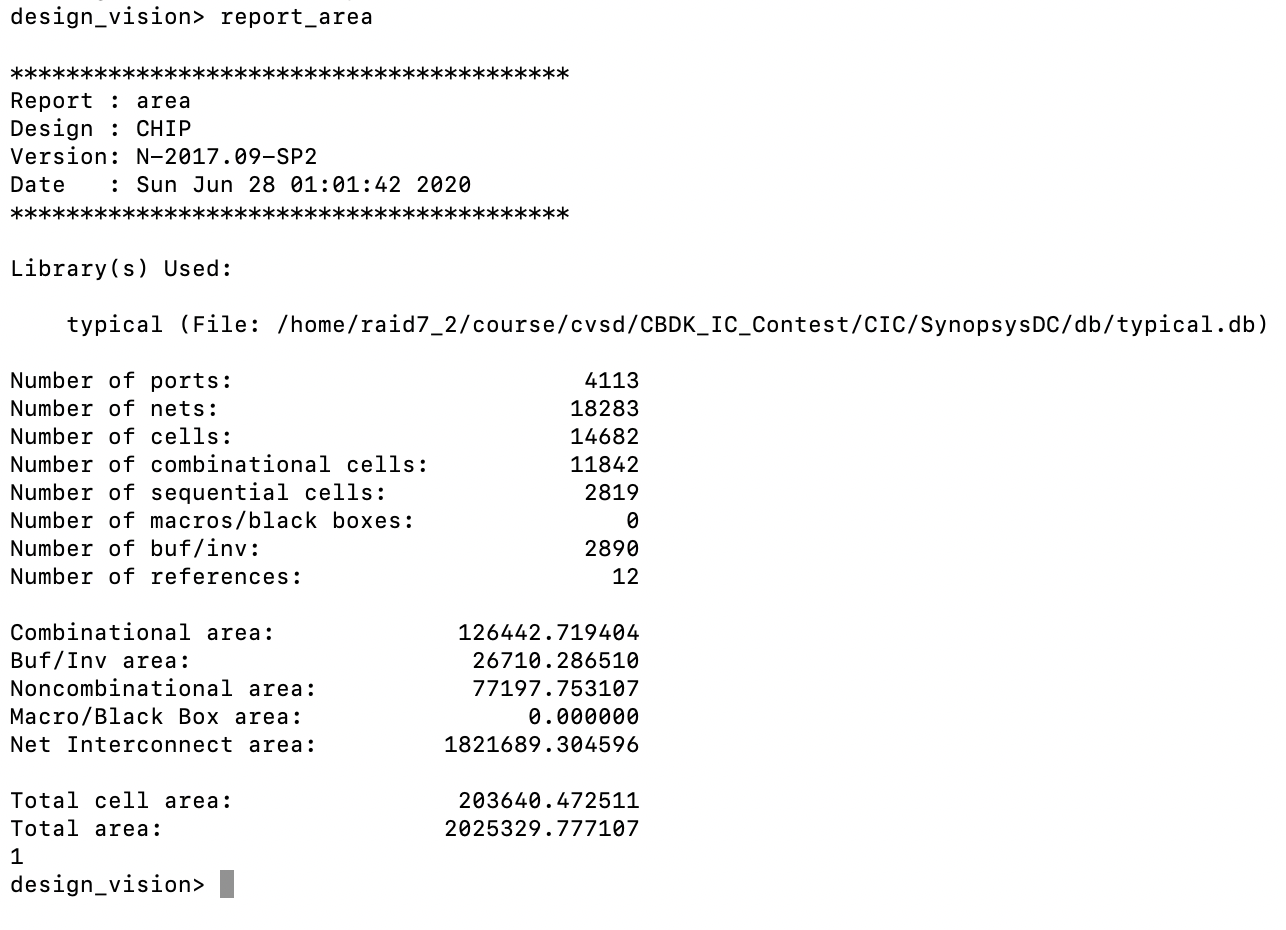
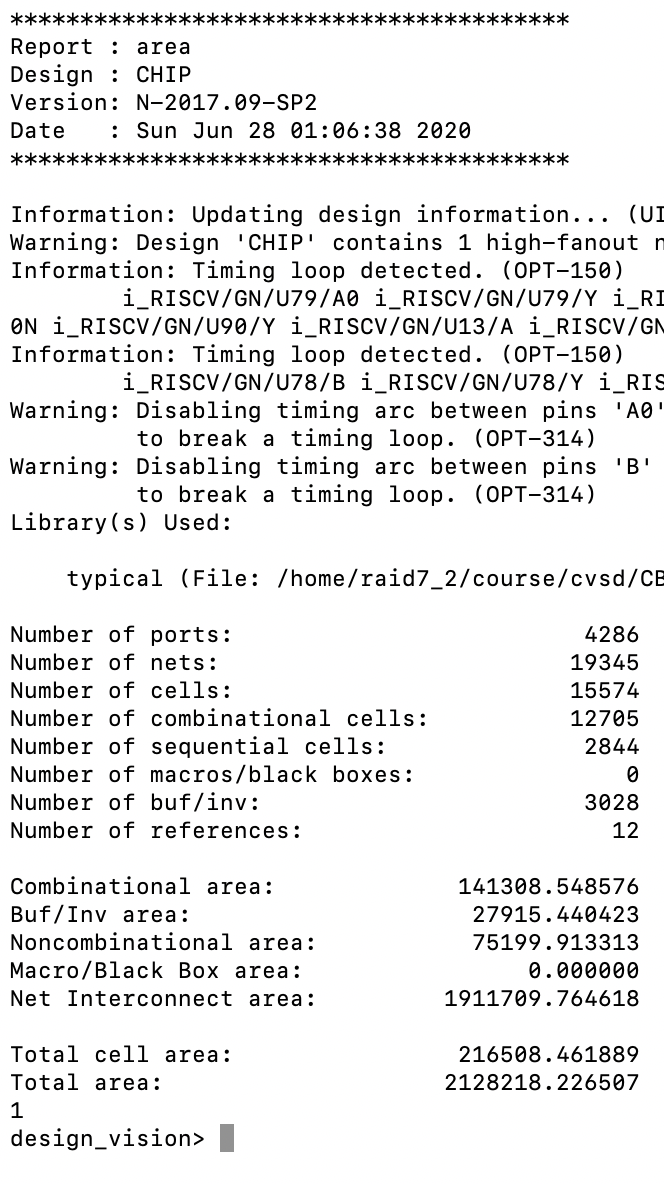
**DSD Final Project Scores (RISC-V)**

**4. Compressed instructions**

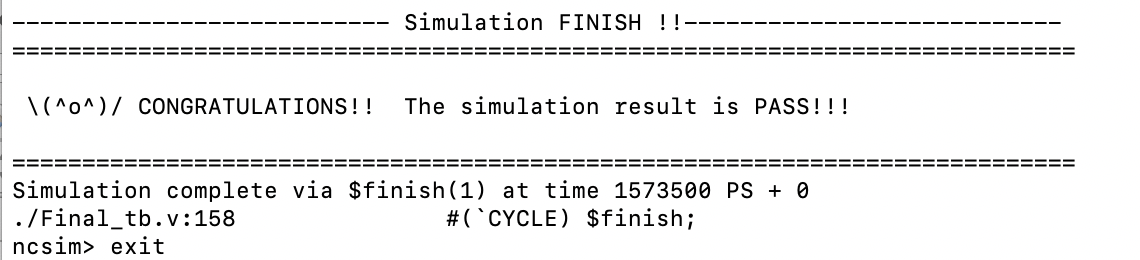
(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2)



216,508.5-203,640.5 = 12,868.0 (um2)

Both of design use non-blocking cache, with synthesis cycle = 3ns.

(2) Total Simulation Time of given I\_mem\_compression: (ns)



Simulation Time : 1,573.5 (ns)

(3) Area\*Total Simulation Time: (um2 \* ns)

AT = 340,676,124.8 (um2 \* ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

3 ns